S/N 10/728,616

OKAY TO ENTER K.N. 04/08/05

IN THE SPECIFICATION

On page 2 first line please insert -- This is a Divisional Application of Serial No.: 10/600,203 filed June 20, 2003, which is presently pending. --

IN THE CLAIMS

Please cancel claims 1-17 and 26-29 without prejudice.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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K.N. 04/08/05

METHOD OF FORMING A STACKED DEVICE FILLER

-- This is a Divisional Application of Serial No. 10/600,203 filed June 20, 2003, which is pending. --

BACKGROUND

In the manufacture of microelectronic devices, packaging density is becoming increasingly important. Stacking of the dice of a multi-processor microelectronic device is one way to improve the packaging density of a microelectronic device. Stacked microelectronic devices are typically formed by stacking two or more wafers with integrated circuitry formed thereon, forming bonded wafers, and then dicing the stacked wafers into individual stacked devices. FIG. 5 illustrates a stacked microelectronic device 236, which may result from the fabrication technique briefly described above. Device 236 comprises a first microelectronic die 216 having an active surface 218, and an integrated circuitry layer 222, which contains integrated circuitry not shown in detail. Typically, the integrated circuitry layer is formed to a depth of approximately 10 microns. An interconnect layer 224 is formed on the die 216, and is illustrated as a plurality of interconnect structures, but may additionally comprise multiple layers of conductive traces separated by dielectric material (not shown). The interconnect layer 224 provides routes for electrical communication between integrated circuits, integrated circuit components, and external devices, for example.

Device 236 comprises a second microelectronic die 202, which additionally contains an integrated circuitry layer 208 and an interconnect layer 212. The physical attachment of interconnect layer 224 to interconnect layer 212 may electrically interconnect integrated circuitry layer 222 with integrated circuitry layer